

Amendments to the claims:

1 (Currently Amended) A digital gain control system
5 comprising:

an rms voltage converter receiving one or more digital
inputs and forming an rms value;

a digital gain controller including having:

an iteration variable set to an initial value;

10 a digital gain value having n data bits, said
digital gain value having a maximum value and a minimum
value, the initial digital gain value being set to the
median of said maximum value and said minimum value;

15 a correction value having an initial value which
is half of said initial digital gain value;

an iteration controller which performs the
following sequential steps m times, said m being an
integer less than said n:

20 comparing the rms value from said rms voltage
converter to a threshold voltage value;

adding said correction value to said digital gain
value if said rms value is less than said threshold
voltage value, or subtracting a said correction value
from said digital gain value if said rms value is
25 greater than said threshold voltage value;

forming a new correction value for a subsequent iteration by halving said correction value.

2 (Previously Amended) The digital gain control system
5 of claim 1 wherein said m is a system constant derived from:

N_{binary} , the number of search bits;

η , the dB/step gain of a receiver to be controlled by said digital gain value;

N_{data} , the bitwidth of the output of an A/D converter
10 sampling a signal amplified by a variable gain amplifier, said variable gain controlled by said digital gain value;

κ , the number of A/D converters quantization steps required for digital signal processing.

15 3 (Previously Amended) The digital gain control system of claim 2 wherein said m is computed from:

$$m = N_{\text{binary}} - \lceil \log_2(10 * \log_{10}((2^{N_{\text{data}}} - 1) / \kappa \eta) + 1) \rceil,$$

and the operator $\lceil . \rceil$ rounds down to an integer value.

20 4 (Previously Amended) The digital gain control system of claim 1 wherein said correction value is $2^{(n-k-1)}$, and said k is the number of times said iteration has been performed.

5 (Previously Amended) The digital gain control system
25 of claim 1 wherein said correction value is positive.

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6 (Previously Amended) The digital gain control system
of claim 1 wherein said correction value is negative.

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7 (Previously Amended) The digital gain control system
of claim 1 wherein said iteration controller operates over a
duration of time substantially equal to the duration of a
received packet, said packet including a first interval and
10 a second interval, the time duration between at least one
said iteration during said first interval being less than
the time duration between at least one said iteration during
said second interval.

15 8 (Previously Amended) The digital gain control system
of claim 7 wherein said first interval corresponds to a
preamble interval of a wireless Ethernet packet.

20 9 (Previously Amended) The digital gain control system
of claim 7 wherein said second interval corresponds to a
payload interval following said first interval in a wireless
Ethernet packet.

10 (Currently Amended) A process for generating a value
25 Vagc where said Vagc is a digital value having n bits and
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operative for controlling the gain of a processor which produces one or more channels of digital samples, said process comprising:

setting Vagc to an initial value;

5 setting Vcorrection to a value substantially equal to half of said Vagc initial value;

performing the following first through fourth steps ~~m times~~ iterations in sequence:

 a first step of measuring said digital samples;

10 a second step of converting ~~of~~ said digital samples into an rms value;

 a third step of comparing said rms value with a threshold value and adding said Vcorrection to said Vagc if said rms value is less than said threshold value, and subtracting said Vcorrection from said Vagc if said rms value is greater than said threshold value;

 a fourth step of forming a new value of said Vcorrection by halving the value of said Vcorrection.

20 11 (Previously Amended) The process of claim 10 wherein said m is a system constant derived from:

 Nbinary, the number of search bits;

η , the dB/step gain of a receiver to be controlled by said digital gain value;

Ndata, the bitwidth of the output of an A/D converter sampling a signal amplified by a variable gain amplifier, said variable gain controlled by said digital gain value;

k, the number of A/D converter quantization steps
5 required for digital signal processing.

12 (Currently Amended) The process of claim 10 wherein said Vagc has a maximum value of $2^{(n-1)} \underline{2^n-1}$.

10 13 (Previously Amended) The process of claim 10 wherein said gain correction value is $2^{(n-k-1)}$, and k is the number of the iteration, starting at 1 and incrementing by 1 for each said iteration.

15 14 (Previously Amended) The process of claim 10 wherein said Vcorrection value is positive.

15 (Previously Amended) The process of claim 10 wherein said Vcorrection value is negative.

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16 (Currently Amended) The process of claim 10 wherein said first through fourth steps comprise an iteration time wherein the iteration time during a first interval is shorter than the iteration time during a second interval and
25 wherein the second interval follows said first interval.

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~~having a first value during a first interval, and said iteration time is longer than said first value during a second interval following said first interval.~~

5 17 (Previously Amended) The process of claim 16 wherein said first interval corresponds to a preamble time T1 of a wireless Ethernet packet.

10 18 (Previously Amended) The process of claim 16 wherein said second interval corresponds to a frame time following the preamble time of a wireless Ethernet packet.

15 19 (Currently Amended) The process of claim 10 wherein said m ~~times~~ iterations occurs during a preamble time of a wireless Ethernet packet.

20 20 (Currently Amended) An RF front end comprising:
an RF receiver responsive to a digital gain control input of width n bits, said RF receiver producing a quadrature output digital values;

a digital gain controller coupled to said digital gain control input and producing a digital output Vagc coupled to said digital gain control input in response to said quadrature output digital values, said output Vagc generated
25 by:

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setting Vagc to an initial value $2^{(n-1)}-1$ and setting an iteration variable k to ± 0 ;

performing the following first through fourth steps while said k is less than m, where said m is an integer less than said n:

a first step of measuring said quadrature output digital values and producing the rms value of said quadrature output digital values;

a second step of comparing said rms value to a threshold value;

a third step of incrementing said k;

a ~~third~~ fourth step of adding a correction value $2^{(n-k-1)}$ to said Vagc if said rms value is less than said threshold value, and subtracting a correction value $2^{(n-k-1)}$ from said Vagc if said rms value is greater than said threshold value. ~~+~~

~~a fourth step of incrementing said k.~~

21 (Currently Amended) The RF front end of claim 20 where wherein said m is a system constant derived from:

Nbinary, the number of search bits;

η , the dB/step gain of a receiver to be controlled by said digital gain value;

Ndata, the bitwidth of the output of an A/D converter sampling a signal amplified by a variable gain amplifier, said variable gain controlled by said digital gain value;

κ, the number of A/D converters quantization steps
5 required for digital signal processing.

22 (Currently Amended) The RF front end of claim 20
~~where~~ wherein said correction value is positive.

10

23 (Currently Amended) The RF front end of claim 20
~~where~~ wherein said correction value is negative.

24 (Currently Amended) The RF front end of claim 20
15 ~~where~~ wherein said first through fourth steps comprise an
iteration time wherein the iteration time during a first
interval is shorter than the iteration time during a second
interval and wherein the second interval follows said first
interval. ~~having a first value during a first interval, and
20 said iteration time is longer than said first value during a
second interval following said first interval..~~

25 (Currently Amended) The RF front end of claim 24
~~where~~ wherein said first interval corresponds to ~~the~~ a
25 preamble time of a wireless Ethernet packet.

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26 (Currently Amended) The RF front end of claim 24
~~where~~ wherein said second interval corresponds to a frame
time following the preamble time of a wireless Ethernet
5 packet.

27 (Currently Amended) The RF front end of claim 20
~~where~~ wherein said m times occurs during a preamble time of
a wireless Ethernet packet.

28 (Currently Amended) A digital gain control system
for a ~~multiplexed stream of first and second~~ stream of
quadrature ~~stream of data,~~ said first and said second stream
15 of quadrature data multiplexed into a single alternating
stream of data, the digital gain control system computing a
gain control value from each said first and said second
stream of quadrature data using a single hardware function
~~comprising two instances of the same function, each said~~
20 ~~instance operating exclusively on either said first or said~~
~~second quadrature stream of data, said function comprising:~~

an rms voltage converter receiving one or more digital
inputs and forming an rms value;

a digital gain controller having:

25 an iteration variable set to an initial value;

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a digital gain value having n bits, said digital gain value having a maximum value and a minimum value, said digital gain value being initially set to the median of said maximum value and said minimum value;

5 a correction value having an initial value which is substantially half of the initial digital gain value;

an iteration process which performs the following sequential steps m times:

10 comparing the rms value from said rms voltage converter to a threshold voltage value;

adding said correction value to said digital gain value if said rms value is less than said threshold voltage level, or subtracting a said correction value from said digital gain value if said rms value is
15 greater than said threshold voltage level;

forming a new ~~said~~ correction value by halving said correction value

whereby said hardware function computes a said digital
20 gain value for each of said first and said second stream of
quadrature data.

29 (Currently Amended) The system of claim 28 ~~where~~
~~said first through fourth steps comprise an iteration time~~
25 wherein the iteration time during a first interval is
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shorter than the iteration time during a second interval and
wherein the second interval follows said first interval.
~~having a first value during a first interval, and said~~
~~iteration time is longer than said first value during a~~
5 ~~second interval following said first interval..~~

10 30 (Previously Amended) The system of claim 28 where
said first interval corresponds to a preamble time of a
wireless Ethernet packet.

 31 (Previously Amended) The system of claim 28 where
said second interval corresponds to a frame time following
the preamble time of a wireless Ethernet packet.

15 32 (Previously Amended) The system of claim 28 where
said m times occurs during a preamble time of a wireless
Ethernet packet.

20 33 (Currently Amended) An RF front end comprising:
a first RF receiver having a digital gain control input
of width n and producing a first quadrature output digital
value including a first I value and a first Q value;

a second RF receiver having a digital gain control input of width n bits and producing a second quadrature output digital value including a second I value and a second Q value;

5 a multiplexer converting said first I value and said second I value into a stream of alternating first and second I values, and also converting said first Q value and said second Q value into a stream of alternating first and second Q values;

10 a digital gain controller coupled to said stream of alternating I values and said stream of alternating Q values and producing a first output Vagc and a second output Vagc, respectively, each of said first Vagc and said second Vagc independently generated by:

15 setting Vagc to an initial value $2^{(n-1)}-1$, where n is said bit width, and setting an iteration variable k to 0;
performing the following steps while said k is less than said m:

a first step of measuring said quadrature digital
20 values and producing the rms value of said quadrature digital values;

a second step of comparing said rms value to a threshold value;

a third step of incrementing said k;

25

a ~~third~~ fourth step of adding a correction value $2^{(n-k-1)}$ to said Vagc if said rms value is less than said threshold value, and subtracting the correction value $2^{(n-k-1)}$ from said Vagc if said rms value is ~~less~~ greater than said threshold value;

~~a fourth step of incrementing said k.~~

34 (Currently Amended) The RF front end of claim 33 ~~where~~ wherein said first through fourth steps comprise an iteration time wherein the iteration time during a first interval is shorter than the iteration time during a second interval and wherein the second interval follows said first interval. ~~having a first value during a first interval, and said iteration time is longer than said first value during a second interval following said first interval..~~

35 (Currently Amended) The RF front end of claim 34 ~~where~~ wherein said first interval corresponds to a preamble time of a wireless Ethernet packet.

36 (Currently Amended) The RF front end of claim 34 ~~where~~ wherein said second interval corresponds to a frame time following the preamble time of a wireless Ethernet packet.

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37 (Currently Amended) The RF front end of claim 34
~~where~~ wherein said ~~m times occurs~~ first through fourth steps
occur during a preamble time of a wireless Ethernet packet.

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38 (Previously Amended) A process for generating a
first value V_{agc} and a second value V_{agc} from an alternating
stream of first quadrature data and second quadrature data,
where said first V_{agc} is derived exclusively from said first
10 quadrature data and said second V_{agc} is derived exclusively
from said second quadrature data, where each of said first
V_{agc} and said second V_{agc} are each digital values having n
bits, said process comprising for each said first and second
V_{agc}:

15 setting V_{agc} to a first value;
 setting V_{correction} to a value equal to substantially
half of said V_{agc} first value;
 performing the following steps m times in sequence:
 measuring one or more said quadrature data samples and
20 converting said quadrature data samples into an rms value;
 comparing said rms value with a threshold value and
 adding said V_{correction} to said V_{agc} if said rms value
is less than said threshold value, and subtracting said
V_{correction} from said V_{agc} if said rms value is greater than
25 said threshold value;

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forming a new value of said Vcorrection by halving the value of said Vcorrection.

39 (Currently Amended) The process of claim 38 ~~where~~
5 wherein said first through fourth steps have an iteration
time wherein the iteration time during a first interval is
shorter than the iteration time during a second interval and
wherein the second interval follows said first interval.
~~with a first value during a first interval, and said~~
10 ~~iteration time is longer than said first value during a~~
~~second interval following said first interval.~~

40 (Currently Amended) The process of claim 38 ~~where~~
wherein said first interval corresponds to a preamble time
15 of a wireless Ethernet packet.

41 (Currently Amended) The process of claim 38 ~~where~~
wherein said second interval corresponds to a frame time
following the preamble time of a wireless Ethernet packet.

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42 (Currently Amended) The process of claim 38 ~~where~~
wherein said m times occurs during a preamble time of a
wireless Ethernet packet.

43 (Previously Presented) The process of claim 1
wherein said m is one of the values 3, 4, or 5.

44 (Previously Presented) The process of claim 11
5 wherein said m is one of the values 3, 4, or 5.

45 (Previously Presented) The process of claim 21
wherein said m is one of the values 3, 4, or 5.

10 46 (Previously Presented) The process of claim 11
whereby said m is computed from:

$$m = N_{\text{binary}} - \lceil \log_2(10 \cdot \log_{10}((2^{N_{\text{data}}}-1)/\kappa\eta) + 1) \rceil$$

and the operator $\lceil \cdot \rceil$ rounds down to an integer value.

15 47 (Previously Presented) The process of claim 21
whereby said m is computed from:

$m = N_{\text{binary}} - \lceil \log_2(10 \cdot \log_{10}((2^{N_{\text{data}}}-1)/\kappa\eta) + 1) \rceil$ and the
operator $\lceil \cdot \rceil$ rounds down to an integer value.